Microprocessor Performance

Nelson H. F. Beebe
Center for Scientific Computing
University of Utah
Department of Mathematics
155 S 1400 E
Salt Lake City, UT 84112-0090
USA
http://www.math.utah.edu/~beebe

Architecture books

- Gerry Blaauw and Fred Brooks, Jr., *Computer Architecture: Concepts and Evolution*, Addison-Wesley (1997), ISBN 0-201-10577-8
- John L. Hennessy and David A. Patterson, *Computer Architecture*, Morgan-Kaufman (2002), 3rd edition, ISBN 1-55860-596-7
- Peter Markstein, *IA-64 and elementary functions: speed and precision*, Prentice-Hall (2000), ISBN 0-13-018348-2

Architecture reports and talks

- Nelson H. F. Beebe, *The Impact of Memory and Architecture on Computer Performance* (1994), http://www.math.utah.edu/~beebe/memperf.pdf
- Nelson H. F. Beebe, *Microprocessor overview* (2001), http://www.chpc.utah.edu/cc/talks/beebe

Bibliographies at http://www.math.utah.edu/pub/tex/bib

- cool-chips
- dectechj
- hot-chips
- fparith
- hpj
- ibmjrd and ibmsysj
- intel-ia-64
- intel-tech-j
- microchip
- visual-instruction-set

Benchmark Web sites

- **LINPACK report:**
  http://www.netlib.org/benchmark/performance.ps
  http://www.netlib.org/utk/people/JackDongarra/faq-linpack.html
- **LINPACK selections:**
  http://performance.netlib.org/performance/html/PDSbrowse.html
- **Standard Performance Evaluation Corporation (SPEC):**
  - **http://www.spec.org/**
- **Utah Mathematics Department:**
  http://www.math.utah.edu/pub/benchmarks

Recent developments

- AMD Athlon (1.53GHz)
- Compaq Alpha 21264 EV68 (1.0GHz)
- HP PA-8700 (750MHz)
- HP/Intel IA-64: McKinley (1GHz)
- HP/Compaq merger
- IBM Power4 (1.3GHz)
- Intel Pentium 4 Xeon Foster (2.2GHz) with hyperthreading

Recent developments

- ✔ Intel Pentium 4 (5GHz)
- ✔ Intel Xeon (2.2GHz)
- ✔ GNU/Linux watch commercially available
- ✔ Compaq cancels Alpha
- ✔ Cray cancels MTA-2, and CEO resigns
- ✔ SGI MIPS R14000 (500MHz)
- ✔ Sun Linux product line

Recent developments

- ✔ Sun UltraSPARC III Cu (1.05GHz)
- ✔ Sun UltraSPARC III performance like II, sigh...

Credit: Hammond & Naffziger, ISSCC 2002

Figure omitted for copyright reasons: see page 7 of http://cpus.hp.com/technical_references/McK-IDF-2001.pdf

Credit: Hammond & Naffziger, ISSCC 2002

Figure omitted for copyright reasons: see page 11 of http://cpus.hp.com/technical_references/McK-IDF-2001.pdf

CPU vs memory: performance gap

Credit: Boncz et al, Proc. 25th VLDB Conference, Edinburgh, Scotland, 1999, p. 54

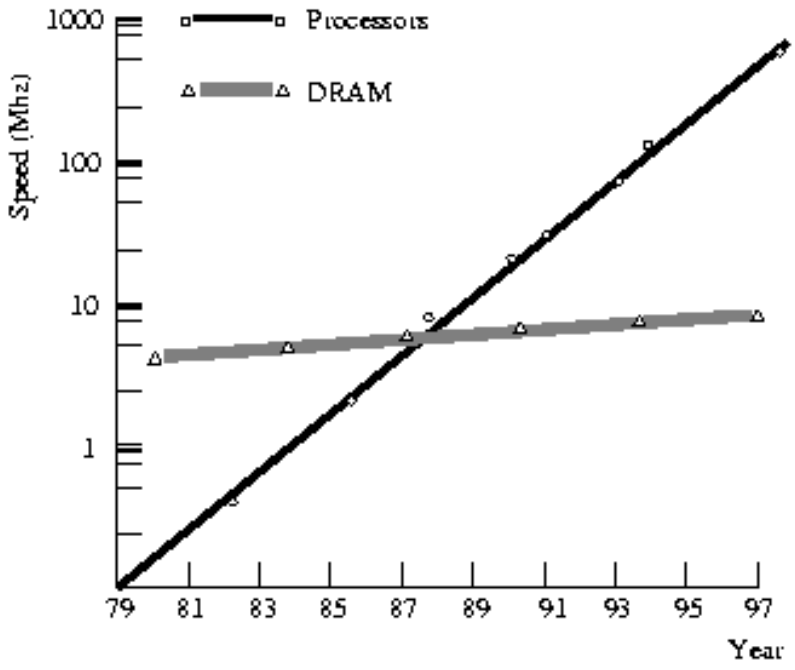

Figure 1: Hardware trends in DRAM and CPU speed

CPU vs memory: performance growth [Credit: H&P CA/2e, Fig 5.1]

Figure omitted for copyright reasons

DRAM access [Credit: H&P, CA/2e, Fig 5.30]

Year	Size	Slowest(ns)	Fastest(ns)	Cycle time
1980	64Kb	180	150	250
1983	256Kb	150	120	220
1986	1Mb	120	100	190
1989	4Mb	100	80	165
1992	16Mb	80	60	120
1995	64Mb	65	50	90

lmbench memory performance on Sun SPARC models

CPU	MHz	Register	L1	L2	RAM
10/412	40	1	2.0	15.7	16.2
20/512	50	1	2.0	8.2	55.8
LX	50	1	2.0	9.8	10.2
US170	167	1	2.0	8.0	47.3
E250	300	1	1.8	9.9	79.5
E5500	400	1	1.6	10.0	102.8

Cache miss rates vs cache size [Credit: H&P CA/2e, Fig 5.23]

Figure omitted for copyright reasons

http://cpus.hp.com/images/die_photos/mckinley_arrows.jpg

Figure omitted for copyright reasons

http://cpus.hp.com/images/die_photos/pa8700.jpg

Figure omitted for copyright reasons

Silicon zoo: MIPS R12000
http://micro.magnet.fsu.edu/creatures

Figure omitted for copyright reasons

LINPACK data

CPU	MHz	N=100	N=1000	Peak
IBM Power4	1300	1074	2894	5200
Itanium	800	n/a	2282	3200
HP PA-8750	750	669	2099	3000
AMD Athlon	1400	705	n/a	2800
Intel P4	2200	1033	1911	2200
Alpha	1000	824	1542	2000
IBM Power3	450	503	1451	1800

LINPACK data

CPU	MHz	N=100	N=1000	Peak
UltraSPARC	450	208	607	900
MIPS R12K	360	170	n/a	720
Intel P2 Xeon	450	98	295	450
Intel P2	333	69	n/a	333

Floating-point developments

- ✔ IEEE 754 committee working on revision of floating-point arithmetic standard
- ✔ IEEE 754 test software site at http://www.math.utah.edu/~beebe/software/ieee
- ✔ extended high-order calculator (hoc v7) with IEEE 754 functions
- ✔ Java floating-point model relaxed

The End